CYII4SC014KAA-GTC
CYII4SM014KAA-GEC

IBIS4-14000 14-Megapixel CMOS Image Sensor

Features

The IBIS4-14000 is a CMOS active pixel image sensor that is comprised of 14 MegaPixels with 3048 x 4560 active pixels on an 8m pitch. The sensor has a focal plane array of 36 x 24mm^2 and operates in rolling shutter mode. At 15 MHz, 3 fps are achieved at full resolution. On-chip FPN correction is available

The pixel design is based on the high-fill-factor active pixel sensor technology of Cypress Semiconductor Corporation (US patent No. 6,225,670 and others). The sensor is available in a monochrome version and a Bayer (RGB) patterned color filter array.

This data sheet allows the user to develop a camera system based on the described timing and interfacing.

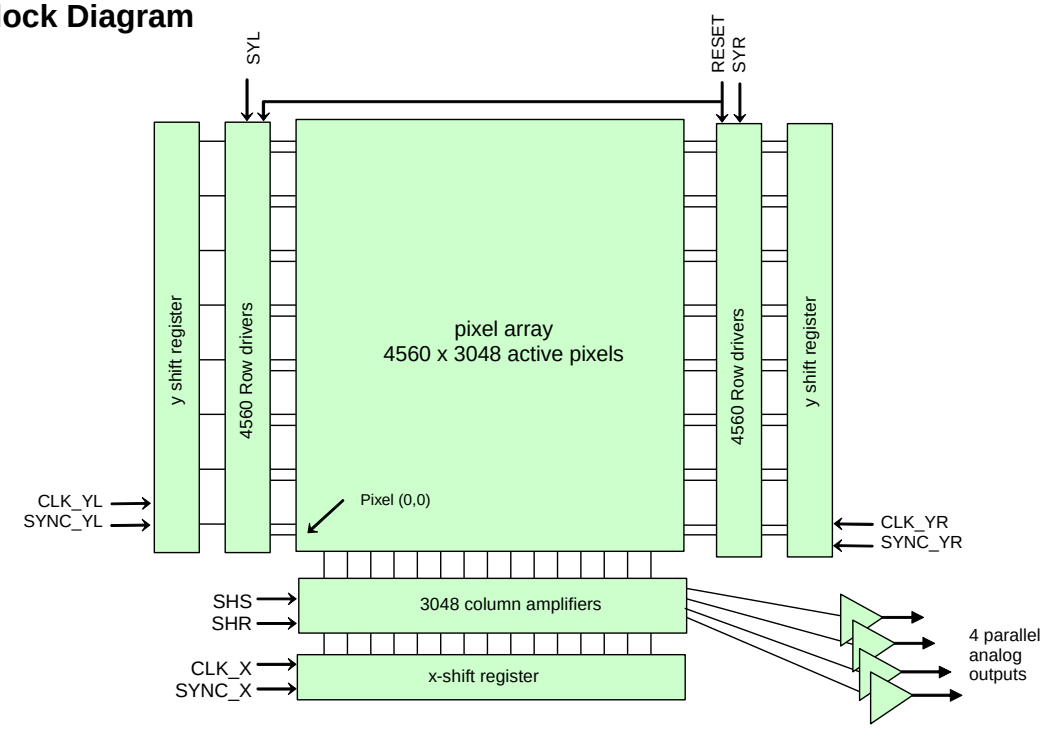
Applications

- Digital photography
- Document scanning
- Biometrics

Table 1. Key Performance Parameters

Parameter	Typical Value
Active Pixels	3048 (H) x 4560 (V)
Pixel Size	8 μm x 8 μm
Optical format	35 mm
Shutter Type	Rolling Shutter
Master Clock	15 MHz
Frame rate	3 fps at full resolution
Sensitivity (@ 650 nm)	1256 V.m^2/W.s
Full Well Charge	65.000 e-
kTC Noise	35 e-
Dark current	223 e-/s
Dynamic Range	65.4 dB
Supply Voltage	3.3V
Power Consumption	< 176 mW
Color Filter Array	Mono and RGB
Packaging	49-pins PGA

Logic Block Diagram



Architecture and Operation

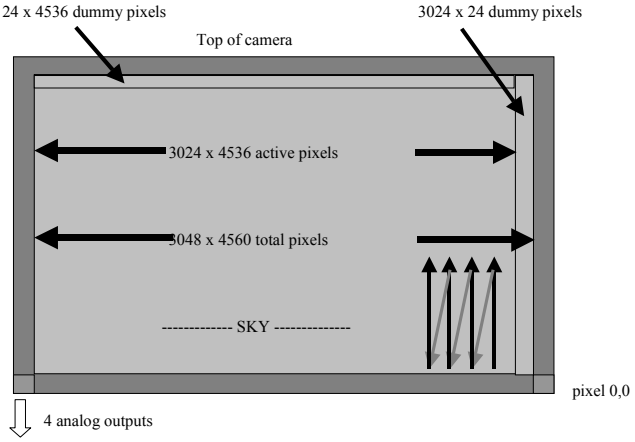
Floor Plan

The basic architecture of the sensor is shown in the Logic Block Diagram on page 1. The Y shift registers point at a row of imager arrays. The imager arrays row is selected by the row drivers or reset by them. There are two Y shift registers, one points at the row that is read out and the other points at the row to be reset. The second pointer may lead the first pointer by a specific number of rows. In that case, the time difference between both pointers is the integration time. Alternatively, both shift registers can point at the same row for reset and readout for a faster reset sequence. When the row is read out, it is also reset. This is to do double sampling for fixed pattern noise reduction.

The pixel array of the IBIS4-14000 consists of 4536 x 3024 active pixels and 24 additional columns and rows which can be addressed (see Figure 1). The column amplifiers read out the pixel information and perform the double sampling operation. They also multiplex the signals on the readout buses which are buffered by the output amplifiers.

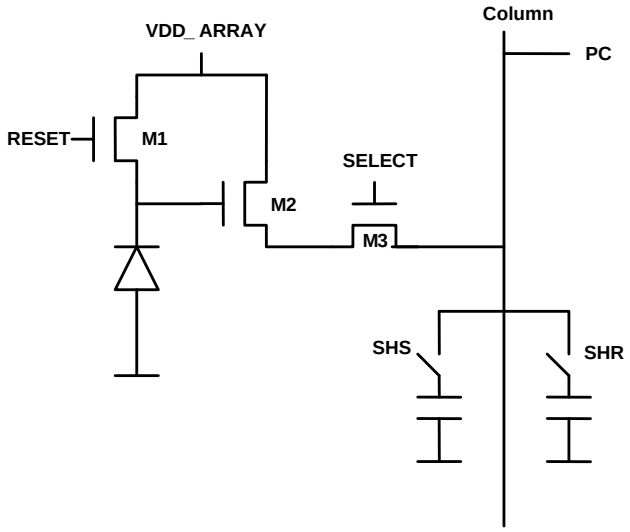
The shift registers can be configured for various subsampling modes. The output amplifiers can be individually powered down and some other extra functions are available. These options are configurable via a serial input port.

Figure 1. Location of the 24 Additional Columns and Rows, Scan Direction of the Array



Pixel Specifications

Figure 2. Pixel and Column Structure Schematic



Architecture

The pixel is a classic three transistor active pixel. The photodiode is a high-fill-factor n-well/p-substrate diode. The chip has separate power supplies for the following:

- General power supply for the analog image core (VDD)
- Power supply for the reset line drivers (VDDR)
- Separate power supply for the pixel itself (VDDARRAY).

FPN and PRNU

Fixed Pattern Noise correction is done on-chip using the Double Sampling technique. The pixel is read out and this voltage value is sampled on the capacitor SHS. After read out the pixel is reset again and this value is sampled by SHR. Both sample and reset values of each pixel are subtracted in the column amplifiers to subtract FPN. Raw images taken by the sensor typically feature a residual (local) FPN of 0.11% RMS of the saturation voltage.

The Photo Response Non Uniformity (PRNU), caused by mismatch of photodiode node capacitances, is not corrected on-chip. Measurements indicate that the typical PRNU is less than1% RMS of the signal level.

Color Filter Array (CFA)

Figure 3. Color Filter Arrangement on the Pixels

The IBIS4-14000 can also be processed with a Bayer RGB color pattern. Pixel (0,0) has a green filter and is situated on a green-red row.

Figure 4 shows the response of the color filter array as a function of the wavelength. Note that this response curve includes the optical cross talk and the NIR filter of the color glass lid as well (see "Cover Glass" on page 24 for response of the color glass lid).

Output Stage

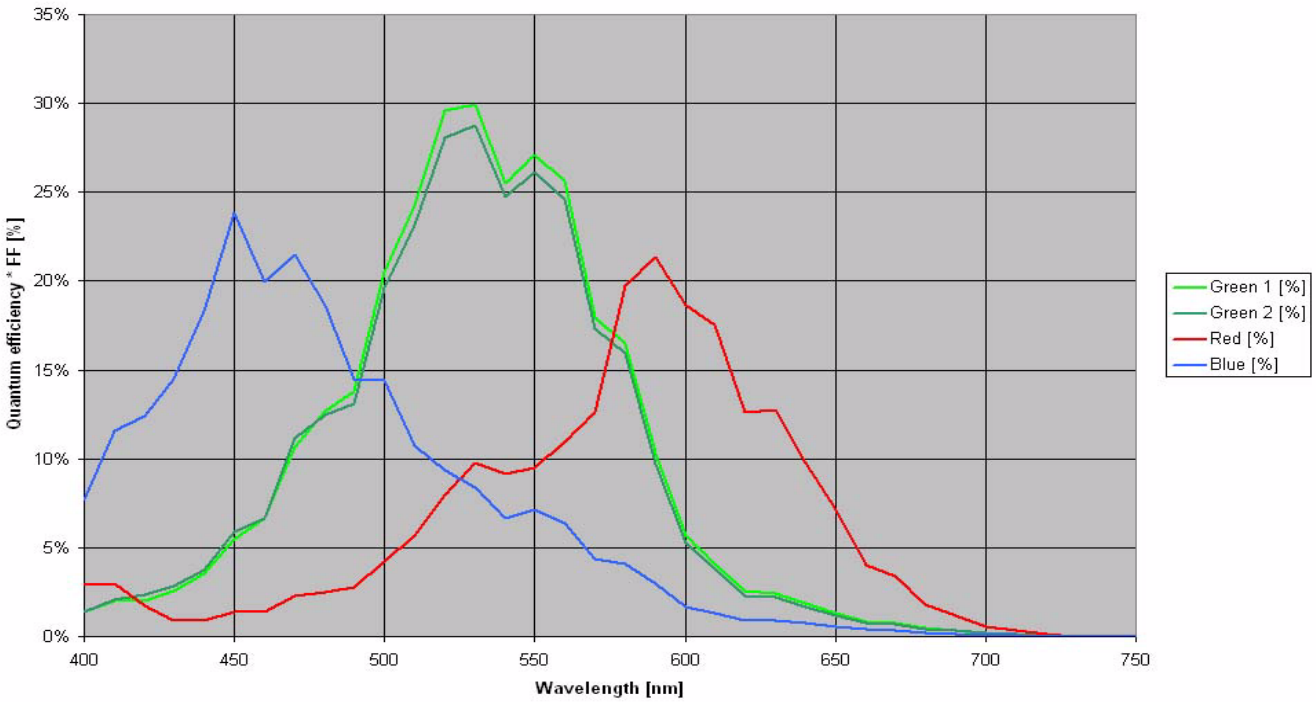
Unity gain buffers are implemented as output amplifiers. These amplifiers can be directly DC-coupled to the analog-digital converter or coupled to an external programmable gain amplifier.

The (dark reference) offset of the output signal is adjustable between 1.7V and 3V. The amplifier output signal is negative going with increasing light levels, with a max. amplitude of 1.2V (at 4V reset voltage, in hard reset mode). The output signal range of the output amplifiers is between 0.5V and 3V.

Notes on analog video signal and output amplifier specifications:

- Video polarity: the video signal is negative going with increasing light level.
- Signal offset: the analog offset of the video signal is settable by an external DC bias (pin 12 DARKREF). The settable range is between 1.7V and 3V, with 2.65V being the nominal expected set point. Hence, the output range (including 1.2V video signal) is between 3V and 0.5V.
- Power control: the output amplifiers can be switched between an "operating" mode and a "standby" mode via the serial port of the imager (see "SPI Register " on page 12 for the configuration).
- Coupling: the IBIS4-14000 can be DC- or AC-coupled to the AD converter.

Figure 4. Color Filter Response Curve

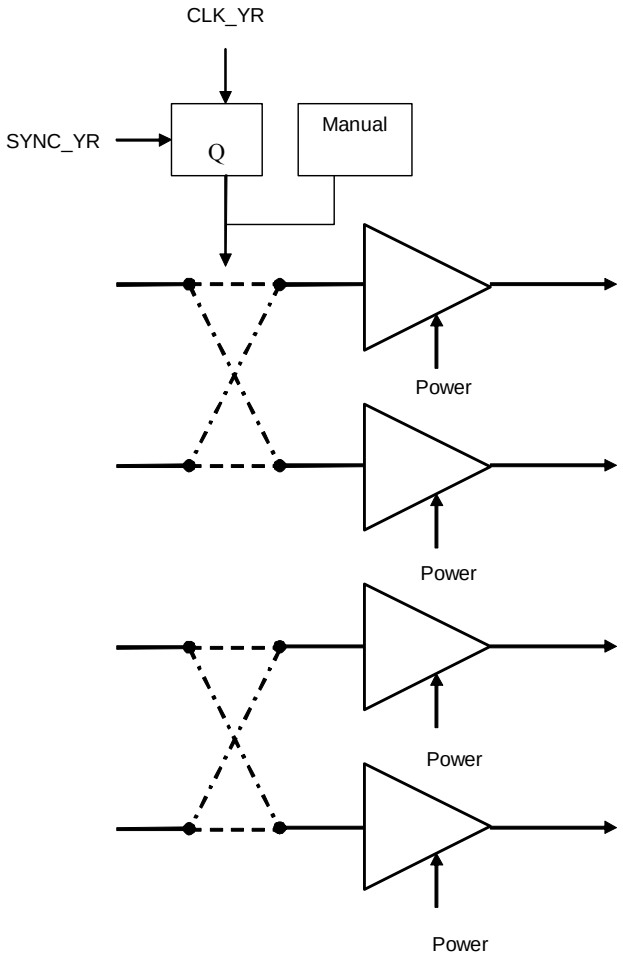


Output Amplifier Crossbar Switch (multiplexer)

A crossbar switch is available that routes the green pixels always to the same output (this is useful for a color device to avoid gain and offset differences between green pixels). The switch can be controlled automatically (with a toggle on every CLK_Y rising edge) or manually (through the SPI register).

A pulse on SYNC_Y resets the crossbar switch. The initial state after reset of the switchboard is read from the SPI control register. When the automatic toggling of the switchboard is enabled, it toggles on every rising edge of the CLK_Y clock. Separate pins are used for the SYNC_Y and CLK_Y signals on the crossbar logic these pins can be connected to the SYNC_YL and CLK_YL pins of the shift register that is used for readout as shown in Figure 5.

Figure 5. Output Amplifier Crossbar Switch



Readout and Subsampling Modes

The subsampling modes available on the IBIS4-14000 are summarized in Table 2.

Table 2. Subsampling Modes

Subsampling Modes Programmed into SPI Register		
X shift register subsampling settings		
Bit-code	**Mode**	**Use**
000 001 010	1:1 Full resolution (all columns)	Full resolution (4 outputs) 4:1 subsampling
011	24:1 Select 4 columns/ skip 20	24:1 subsampling (2 outputs)
100	8:1 Select 4 columns / skip 4s	8:1 subsampling (2 outputs)
101	12:1 Select 4 columns / skip 8	12:1 subsampling (2 outputs)
Y shift register subsampling settings		
Bit-code	**Mode**	**Use**
000 010 100	4:1 Select 2 rows / skip 2	4:1 subsampling
001	1:1 Full resolution (all rows)	Full resolution
011	6:1 Select 2 rows / skip 4	6:1 subsampling
101	12:1 Select 2 rows / skip 10	12:1 subsampling

Each mode is selected independently for the X and Y shift registers. The subsampling mode is configured via the serial input port of the chip. The Y and X shift registers have some difference in subsampling modes because of constraints in the design of the chip.

The baseline full resolution operation mode uses four outputs to read out the entire image. Four consecutive pixels of a row are put in parallel on the four parallel outputs.

Subsampling is implemented by a shift register with hard coded subsample modes. Depending on the selected mode the shift register skips the required number of pixels when shifting the row or column pointer.

The X shift register always selects four consecutive columns in parallel. You can subsample in X by activating one of the modes wherein a multiple of four consecutive columns are skipped on a CLK_X pulse. The Y shift register selects a single row. It consecutively selects two adjacent rows and then skips a set number of rows (the number of rows to skip is set in the subsample mode).

This implementation is chosen for easy subsampling of color images through a 2-channel readout. This way color data from 2x2 pixels is made available in all subsample modes. On monochrome sensors this is not required, one output can be used and every second row selected by the Y shift register can be skipped. This doubles the frame rate. Note that for 2 or 1 channel readout, you can power down the not-used output amplifiers through the SPI shift register.

Rows can also be skipped by extra CLK_Y pulses. You do not need to apply additional control pulses to rows that are skipped. This is another way to implement extra subsampling schemes. For example, to support the 24:1 X shift register mode vertically, set the Y shift register to the 12:1 mode and given an additional CLK_Y pulse at the start of each row.

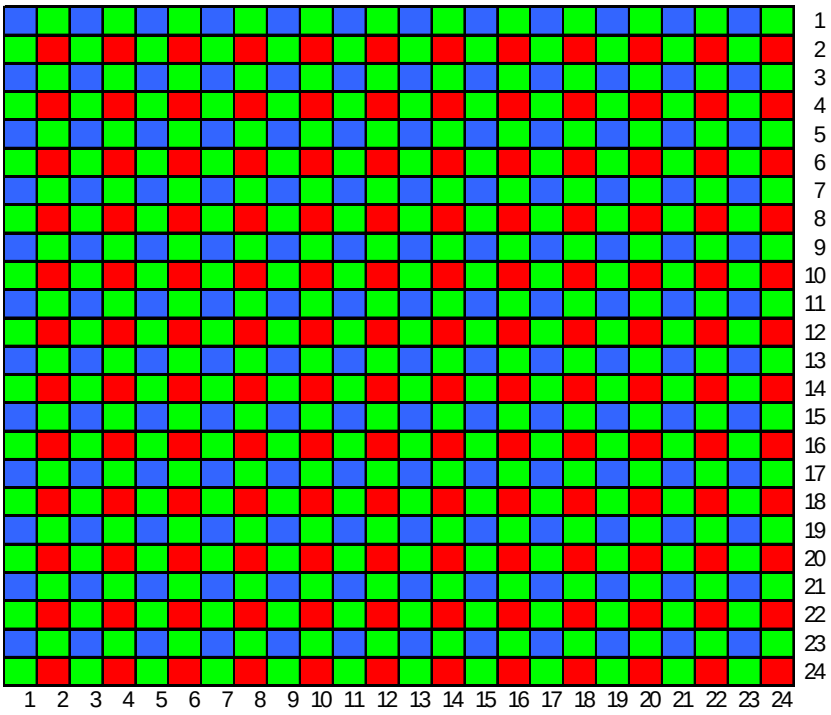
Table 3 lists the frame rates of the IBIS4-14000 in various subsample modes with only one output. The row blanking time (dead time between readout of successive rows) is set to 17.5 s.

Table 3. Frame Rates and Resolution for Various Subsample Modes

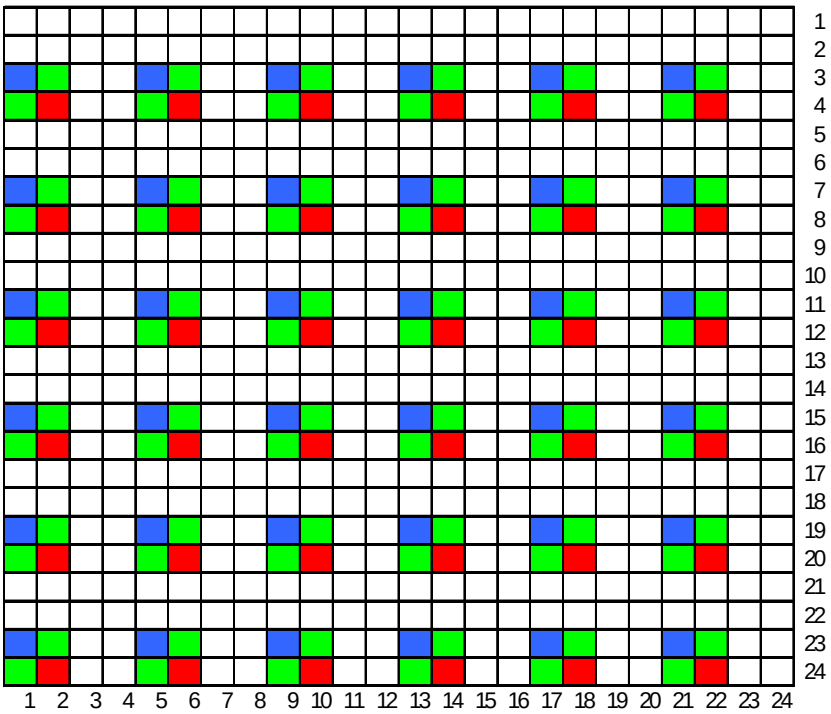
Ratio	# Outputs	Image Resolution	Frame rate [frames/s]	Frame readout time [s]
1:1	4	3024 x 4536	3.25	0.308
4:1	1	756 x 1134	12.99	0.077
8:1	1	378 x 567	41.30	0.024
12:1	1	252 x 378	77.13	0.013

Note The 24 additional columns and rows do not subsample (see Figure 1 on page 2).

Figure 6. B and C Subsample Mode

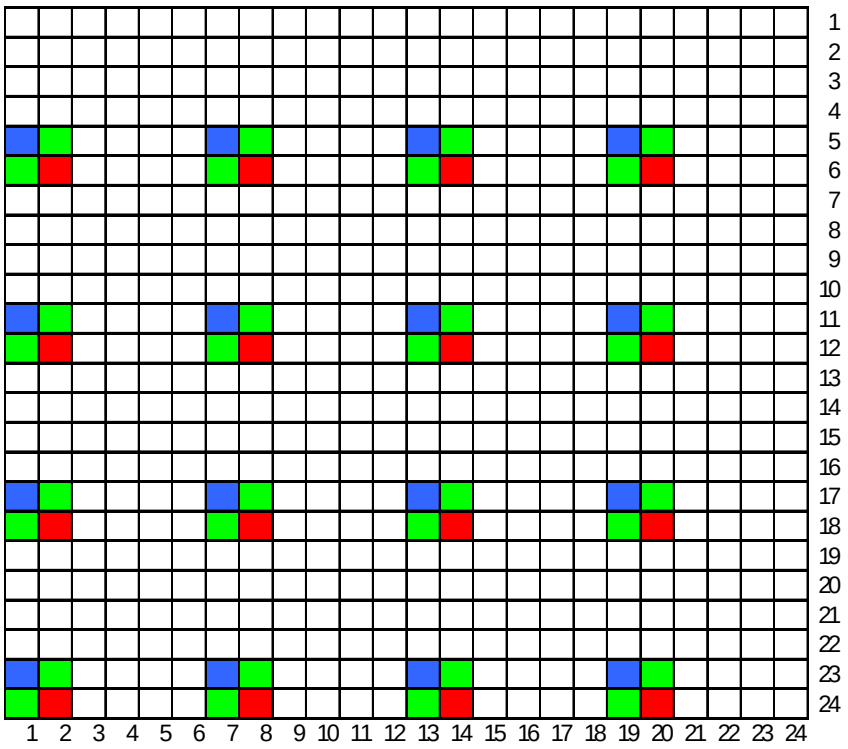


mode B - 1:1

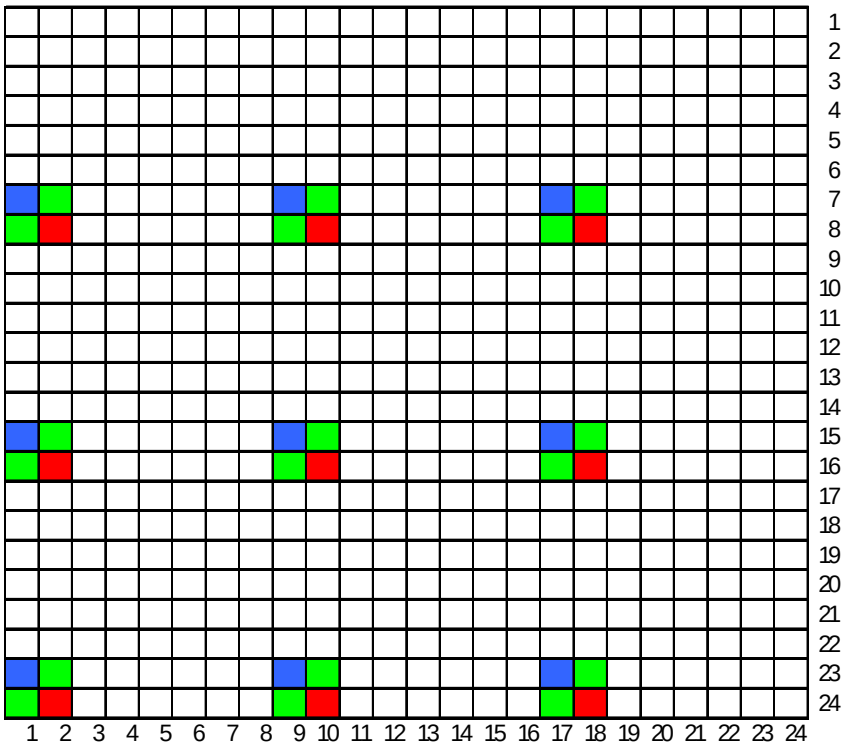


mode C - 1:4

Figure 7. D and E Subsample Mode

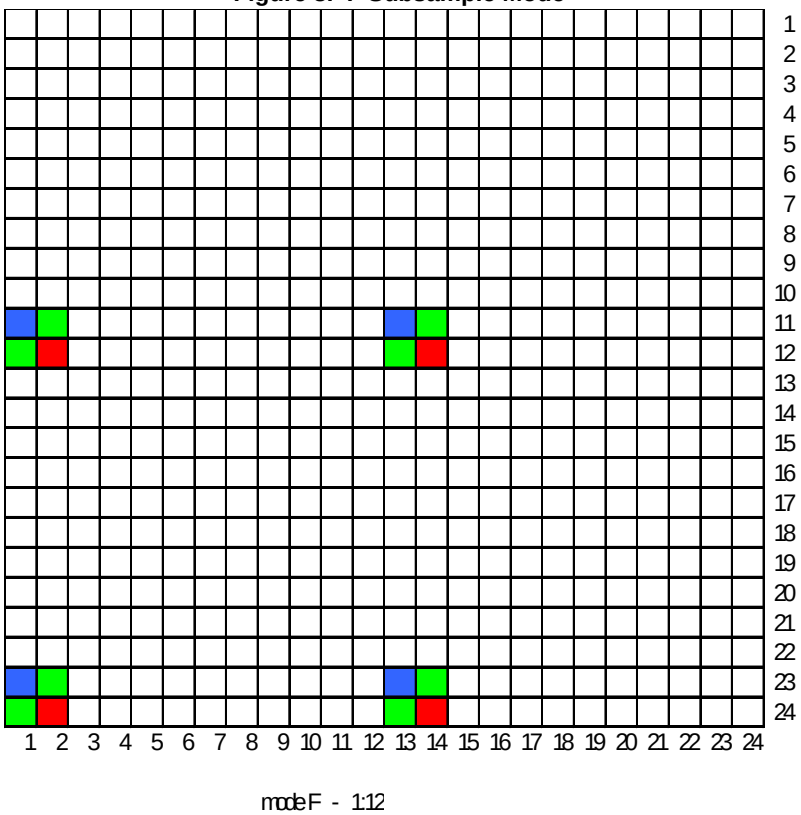


mode D - 1:6



mode E - 1:8

Figure 8. F Subsample Mode



Sensor Read Out Timing Diagrams

Row Sequencer

The row sequencer controls pulses to be given at the start of each new line. Figure 9 on page 9 shows the timing diagram for this sequence.

The signals to be controlled at each row are:

- CLK_YL and CLK_YR: These are the clocks of the YL and YR shift register. They can be driven by the same signals and at a continuous frequency. At every rising edge, a new row is being selected.
- SELECT: This signal connects the pixels of the currently sampled line with the columns. It is important that PC and SELECT are never active together.
- PC: An initialization pulse that needs to be given to precharge the column.
- SHS (Sample & Hold pixel Signal): This signal controls the track and hold circuits in the column amplifiers. It is used to sample the pixel signal in the columns. (0 = track ; 1 = hold).
- RESET: This pulse resets the pixels of the row that is currently being selected. In rolling shutter mode, the RESET signal is pulsed a second time to reset the row selected by the YR shift register. For “reset black” dark reference signals, the reset pulse can be pulsed also during the first PC pulse. Normally, the rising edge of RESET and the falling edge of PC occur at the same position. The falling edge of RESET lags behind the rising PC edge.
- SHR (Sample & Hold pixel Reset level): This signal controls another track and hold circuit in the column amplifiers. It is used to sample the pixel reset level in the columns (for double sampling). (0 = track ; 1 = hold).
- SYL (Select YL register): Selects the YL shift register to drive the reset line of the pixel array.
- SYR (Select YR register): Selects the YR shift register to drive the reset line of the pixel array. For rolling shutter applications, SYL and SYR are complementary. In full frame readout, both registers may be selected together, only if it is guaranteed that both shift registers point to the same row. This can reduce the row blanking time.
- SYNC_YR and SYNC_YL: Synchronization pulse for the YR and YL shift registers. The SYNC_YR/SYNC_YL signal is clocked in during a rising edge on CLK_YR/CLK_YL and resets the YR/YL shift register to the first row. Both pulses are pulsed only once each frame. The exact pulsing scheme depends on the mode of use (full frame/ rolling shutter). A 200 ns setup time applies. See Table 4 on page 9.
- SYNC_X: Resets the column pointer to the first row. This has to be done before the end of the first PC pulse in case the previous line has not been read out completely.

Figure 9 on page 9 shows the basic timing diagram of the IBIS4-14000 image sensor and Table 4 on page 9 shows the timing specifications of the clocking scheme.

Figure 9. Line Read Out Timing

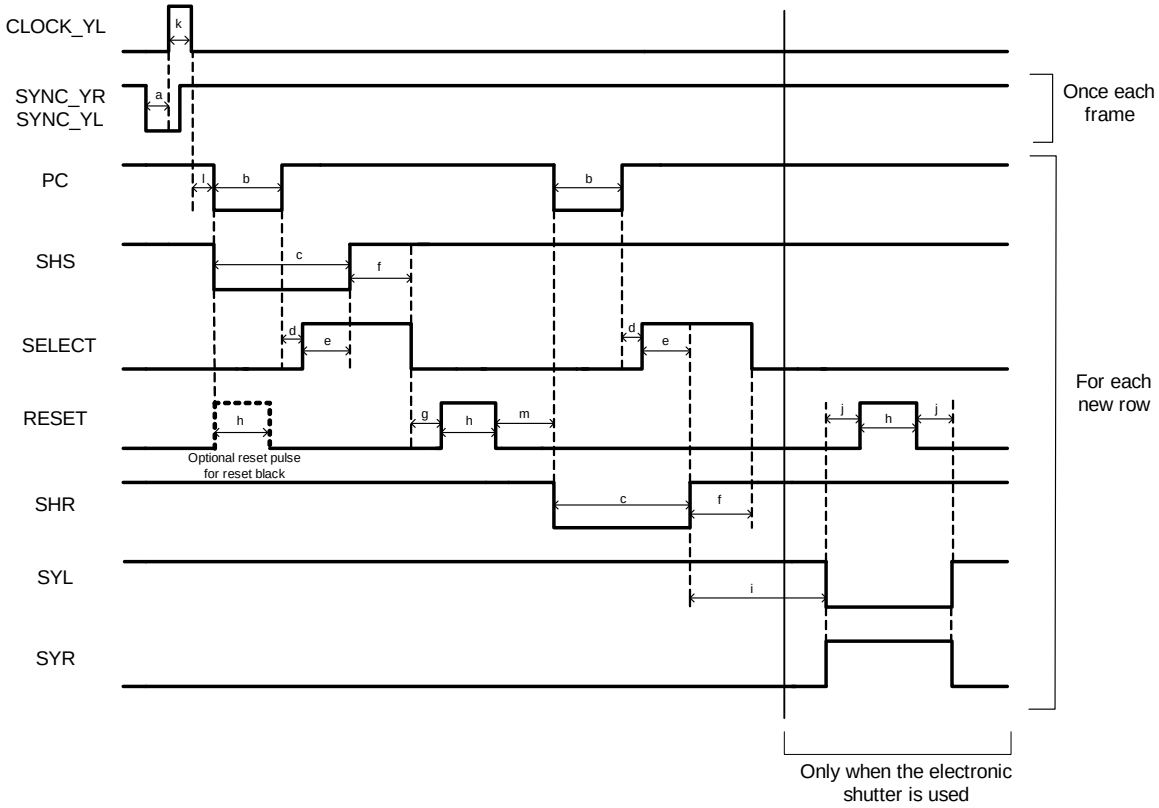


Table 4. Timing Constraints for the Row Sequencer

Symbol	Min	Typ.	Description
a	200 ns	600 ns	Min. SYNC set-up times. SYNC_Y is clocked in on rising edge on CLK_Y. SYNC_Y pulse must overlap CLK_Y by one clock period. Setup times of 200 ns apply after SYNC edges. Within this setup time no rising CLK edge may occur.
b		2.7 µs	Duration of PC pulse.
c		10 µs	Delay between falling edge on PC and rising edge on SHS/SHR. Duration of SHS/SHR pulse.
d		1.3 µs	Delay between rising edge on PC and rising edge on SELECT.
e		6.5 µs	Delay between rising edge on SELECT and rising edge on SHS/SHR.
f		100 ns	Delay between rising edge on SHS and falling edge on SELECT.
g		1.4 µs	Delay between falling edge of SELECT and rising edge of RESET.
h		5 µs	Duration of RESET pulse.
i		1.28 µs	Delay between rising edge on SHR and rising edge on SYR.
j	h+2*CLK	500 ns	SYL and SYR pulses must overlap second RESET pulse at both sides by one clock cycle.
k		240 ns	Duration of CLOCK_Y pulse.
l		3µs	Delay between falling edge of CLK_Y and Falling edge of PC and SHS.
m		500ns	Delay between falling edge of RESET and falling edge of PC and SHR.

Notes CLK = one clock period of the master clock, shortest system time period available.

In the Figure 9 on page 9 timing diagram, the YR shift register is used for the electronic shutter. The CLK_YR is driven identically as CLK_YL. The SYNC_YR pulse leads the SYNC_YL pulse by a given number of rows. Relative to the row timing, both SYNC pulses are given at the same time position.

SYNC_YR and SYNC_YL are only pulsed once each frame, SYNC_YL is pulsed when the first row is read out and SYNC_YR is pulsed for the electronic shutter at the appropriate moment.

This timing assumes that the registers that control the subsampling modes have been loaded in advance (through the SPI interface), before the pulse on SYNC_YL or SYNC_YR.

The second reset pulse and the pulses on SYL and SYR (all pulses drawn in red) are only applied when the rolling electronic shutter is used. For full frame integration, these pulses are skipped.

The SYNC_Y pulse is also used to initialize the switchboard (output multiplexer). This is also done by a synchronous reset on the rising edge of CLK_Y. Normally the switchboard is controlled by the shift register used for readout (this is the YL shift register). This means that pin SYNC_Y can be connected to SYNC_YL, and pin CLK_Y can be connected to CLK_YL.

The additional RESET BLACK pulse (indicated in dashed lines in Figure 9 on page 9) can be given to make one or more lines black. This is useful to generate a dark reference signal.

Timing Pulse Pattern for Readout of a Pixel

Figure 10 shows the timing diagram to preset (sync) the X shift register, read out the image row, and analog-digital conversion. There are 3 tasks:

- Preset the X shift register: Apply a low level to SYNC_X during a rising edge on CLK_X at the start of a new row
- Readout of the image row: Pulse CLK_X
- Analog-digital conversion: Clock the ADC

The SYNC pulses perform a synchronous reset of the shift registers to the first row/column on a rising edge on CLK. This is identical for all shift registers (YR, YL and X).

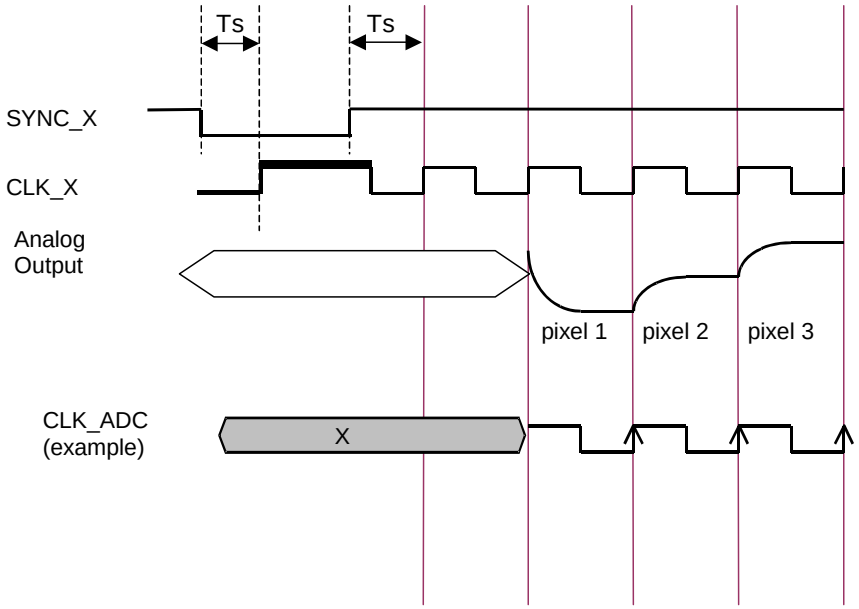
Note The SYNC_X signal has a setup time Ts of 150 ns. For the YR and YS shift registers, the setup time is 200 ns. CLK_X must be stable at least during this setup time.

If a partial row readout is performed, 2 CLK_X pulses (with SYNC_X = LOW) are required to fully deselect the column where the X pointer is stopped. A single CLK_X leaves the column partially selected which then has a different response when read out in the next row.

When full row readout is performed, the last column is fully deselected by a single CLK_X pulse (with SYNC_X = LOW). The X-register is reset by a single CLK_X pulse (with SYNC_X = LOW). In case of partial row readout, give the SYNC_X pulse before the sample pulses (SHR and SHS) of the process to avoid a different response of the last column of the previous window.

For the X shift register the analog signal is delayed by 2 clock periods before it becomes available at the output (due to internal processing of the signal in the columns and output amplifier). Figure 10 gives an example of an ADC clock for an ADC that samples on the rising edge.

Figure 10. Row Readout Timing Sequence



Fast Frame Reset Timing Diagram

Figure 11 shows the reset timing for a fast frame reset.

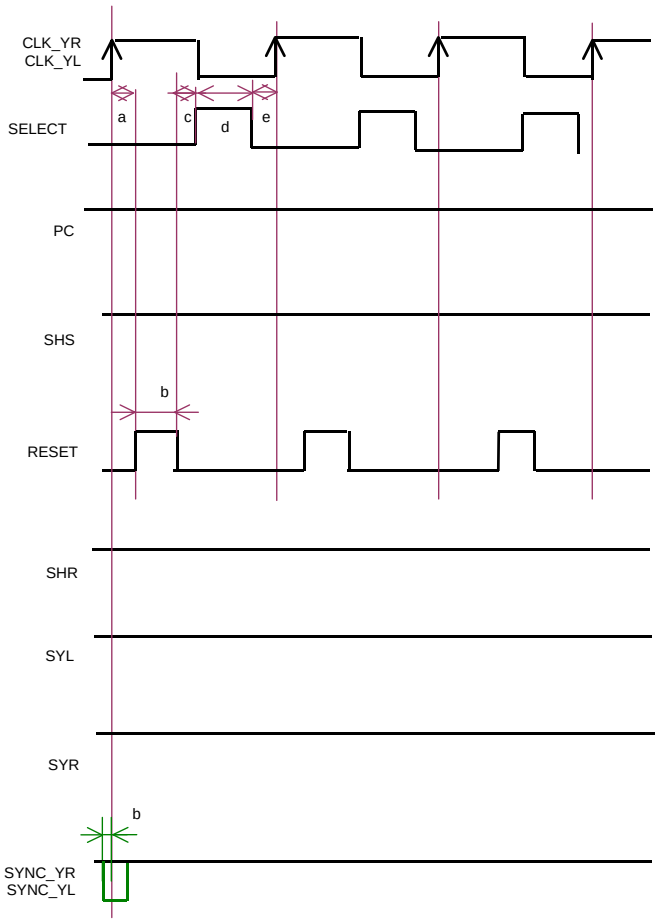
Keep both SYL and SYR high to speed up the reset mechanism and reduce propagation delays. PC, SHS, SHR can be kept high since they do not interact with the pixel reset mechanism.

Table 5 lists the timing specifications for RESET, CLK_Y and SELECT.

Table 5. Fast Reset Timing Constraints

Symbol	Typical	Description
a	0 µs	Delay between rising CLK_Y edge and Reset.
b	4 µs	Reset pulse width.
c	0	Reset hold time.
d	1.6 µs	Select pulse width.
e	1 µs	Setup hold time. CONSTRAINT: a + e > 1 us due to propagation delay on pixel select line.

Figure 11. Fast Reset Sequence Timing



SPI Register

SPI Interface Architecture

The elementary unit cell of the serial to parallel interface consists of two D-flip-flops. The architecture is shown in Figure 12. 16 of these cells are connected in parallel, having a common /CS and SCLK form the entire uploadable parameter block, where D_{in} is connected to D_{out} of the next cell. The uploaded settings are applied to the sensor on the rising edge of signal /CS.

Figure 12. SPI Interface

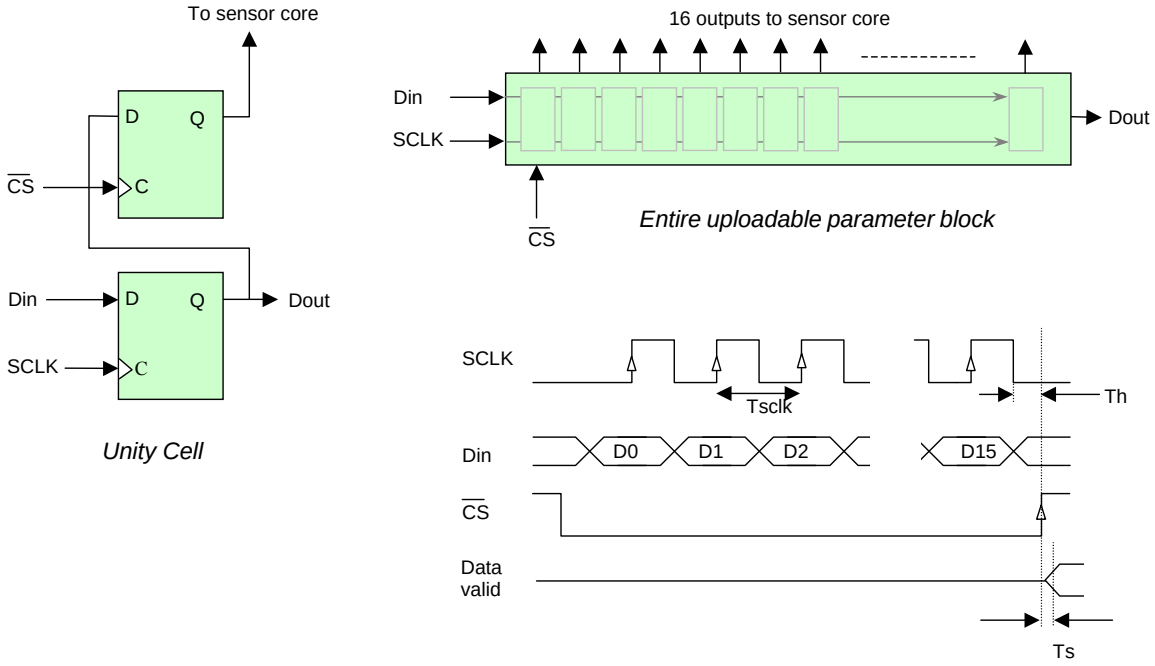


Table 6. Timing Requirements Serial Parallel Interface

Parameter	Value
Tsclk	100 ns
Ts	50 ns
Th	50 ns

SPI Register Definition

Sensor parameters can be serially uploaded inside the sensor at the start of a frame. The parameters are:

- Subsampling modes for X and Y shift registers (3-bit code for six subsampling modes)
- Power control of the output amplifiers, column amps and pixel array. Each amplifier can be individually powered up/down
- Output crossbar switch control bits. The crossbar switch is used to route the green pixels to the same output amplifiers at all times. A first bit controls the crossbar. When a second bit is set, the first bit toggles on every CLK_Y edge to automatically route the green pixels of the bayer filter pattern.

The code is uploaded serially as a 16-bit word (LSB uploaded first).

Table 7 on page 13 lists the register definition. The default code for a full resolution readout is 33342 (decimal) or 1000 0010 0011 1110.

Table 7. Serial Sensor Parameters Register Bit Definitions

BIT	Description'
0 (LSB)	set to zero (0).
1	1 = power on sensor array ; 0 = power-down.
2	1 = power up output amplifier 4; 0 = power-down.
3	1 = power up output amplifier 3; 0 = power-down.
4	1 = power up output amplifier 2; 0 = power-down.
5	1 = power up output amplifier 1; 0 = power-down.
6 7 8	3-bit code for subsampling mode of X shift register: 000 = full resolution 011 = select 4, skip 20 001 = full resolution 100 = select 4, skip 4 010 = full resolution 101 = select 4, skip 8
9 10 11	3-bit code for subsampling mode of Y shift registers: 000 = select 2, skip 2 011 = select 2, skip 4 001 = full resolution 100 = select 2, skip 2 010 = select 2, skip 2 101 = select 2, skip 2
12	Crossbar switch (output multiplexer) control bit initial value. This initial value is clocked into the crossbar switch at a SYNC_YR rising edge pulse (when the array pointers jump back to row 1). The crossbar switch control bit selects the correspondence between multiplexer busses and output amplifiers. Bus-to-output correspondence is according to the following table: **Bus** **when bit set to 0** **when bit set to 1** 1 output 1 output 2 2 output 2 output 1 3 (4 outputs) output 3 output 4 4 (4 outputs) output 4 output 3
13	1 = Toggle crossbar switch control bit on every odd/even line. In order to let green pixels always use the same output amplifier automatically, this bit must be set to 1. On every CLK_Y rising edge (when a new row is selected), the crossbar switch control bit will toggle. Initial value (after SYNC_Y) is set by bit 12.
14	Not used.
15 (MSB)	1 = Power-up sensor array; 0 = Power-down.

Three pins are used for the serial data interface. This interface converts the serial data into an (internal) parallel data bus (Serial-Parallel Interface or SPI). The control lines are:

■ DATA: The data input. LSB is clocked in first.

■ CLK: Clock, on each rising edge, the value of DATA is clocked in

■ CS: Chip select, a rising edge on CS loads the parallelized data into the on-chip register.

The initial state of the register is undefined. However, no state exists that destroys the device.

Pin Configuration

Table 8 lists the pin configuration of the IBIS4-14000. Figure 16 on page 21 shows the assignment of pin numbers on the package.

Table 8. Pinout Configuration

Pin #	Name	Function	Comment
1	OBIAS	Bias current output amplifiers.	Connect with 10kΩ to VDD and decouple with 100 nF to GND.
2	GND	Ground for output 3.	
3	OUT3	Output 3.	
4	GND	Ground for output 4.	
5	OUT4	Output 4.	
6	VDD	Power supply.	Nominal 3.3V
7	GND	Ground.	0V
8	OUT2	Output 2.	
9	GND	Ground for output 2.	
10	OUT1	Output 1.	
11	GND	Ground for output 1.	
12	DARKREF	Offset level of output signal.	Typ. 2.6V. min. 1.7V max. 3V
13	TEMP1	Temperature sensor. Located near the output amplifiers (pixel 4536, 0) near the stitch line).	Any voltage above GND forward biases the diode. Connect to GND if not used.
14	PHDIODE	Photodiode output. Yields the equivalent photocurrent of 250 x 50 pixels. Diode is located right under the pad.	Reverse biased by any voltage above GND Connect to GND if not used.
15	CLK_Y	Y clock for switchboard.	Clocks on rising edge Connect to CLK_YL (or drive identically)
16	SYNC_Y	Y SYNC pulse for switchboard.	Low active: synchronous sync on rising edge of CLK_Y Connect to SYNC_YL (or drive identically)
17	TEMP2	Temperature sensor. Located near pixel (24,0).	Any voltage above GND forward biases the diode. Connect to GND if not used.
18	GNDAB	Anti-blooming reference level (= pin 33).	Typ. 0V. Set to 1.5V for improved anti-blooming.
19	GND	Ground.	0V
20	VDD	Power supply.	Nominal 3.3V
21	VDDR	Power supply for reset line drivers	Nominal 4V Connected on-chip to pin 30
22	CLK_YR	Clock of YR shift register.	Shifts on rising edge.
23	SYR	Activate YR shift register for driving of reset and select line of pixel array.	High active. Exact pulsing pattern see timing diagram. Both SYR = 1 and SYL = 1 is not allowed, except when the same row is selected!
24	SYNC_YR	Sets the YR shift register to row 1.	Low active. Synchronous sync on rising edge of CLK_YR 200 ns setup time
25	VDDARRAY	Pixel array power supply (= pin 26).	3V
26	VDDARRAY	Pixel array power supply (= pin 25).	3V
27	SYNC_YL	Sets the YL shift register to row 1.	Low active. Synchronous sync on rising edge of CLK_YL 200 ns setup time.
28	SYL	Activate YL shift register for driving of reset and select line of pixel array.	High active. Exact pulsing pattern see timing diagram. Both SYR = 1 and SYL = 1 is not allowed, except when the same row is selected.

Table 8. Pinout Configuration(continued)

Pin #	Name	Function	Comment
29	CLK_YL	Clock of YL shift register.	Shifts on rising edge.
30	VDDR	Power supply for reset line drivers.	Nominal 4V. Connected on-chip to pin 21.
31	VDD	Power supply.	Nominal 3.3V
32	GND	Ground.	0V
33	GNDAB	Anti-blooming reference level (= pin 33).	Typ. 0V. Set to 1V for improved anti-blooming.
34	SELECT	Control select line of pixel array.	High active. See timing diagrams.
35	RESET	Reset of the selected row of pixels.	High active. See timing diagrams.
36	CBIAS	Bias current column amplifiers.	Connect with 22 kΩ to VDD and decouple with 100 nF to GND.
37	PCBIAS	Bias current.	Connect with 22 kΩ to VDD and decouple with 100 nF to GND.
38	DIN	Serial data input.	16-bit word. LSB first.
39	SCLK	SPI interface clock.	Shifts on rising edge.
40	CS	Chip select.	Data copied to registers on rising edge.
41	PC	Row initialization pulse.	See timing diagrams.
42	SYNC_X	Sets the X shift register to row 1.	Low active. Synchronous sync on rising edge of CLK_X 150 ns setup time.
43	GND	Ground.	0V
44	VDD	Power supply.	Nominal 3.3V
45	CLK_X	Clock of YR shift register.	Shifts on rising edge.
46	SHR	Row track & hold reset level (1 = hold; 0 = track).	See timing diagram.
47	SHS	Row track & hold signal level (1 = hold; 0 = track).	See timing diagram.
48	XBIAS	Bias current X multiplexer.	Connect with 10 kΩ to VDD and decouple with 100 nF to GND.
49	ABIAS	Bias current pixel array.	Connect with 10 MΩ to VDD and decouple with 100 nF to GND.

Specifications

General Specifications

Table 9. IBIS4-14000 General Specifications

Parameter	Value	Remarks
Pixel architecture	3T pixel	
Technology	CMOS	
Pixel size	8 x 8 μm^2	
Resolution	3048 x 4560	13.9 megapixels
Power supply	3.3V	
Shutter type	Electronic rolling shutter	
Pixel rate	15 MHz nominal	20 MHz with extra power dissipation.
Frame rate	3.25 frames/s	Full resolution with 4 parallel analog outputs @ 15 MHz/channel
Power dissipation	176 mW 53 mA	

Electro-Optical Specifications

Overview

All parameters are measured using the default settings (see recommended operating conditions) unless otherwise specified.

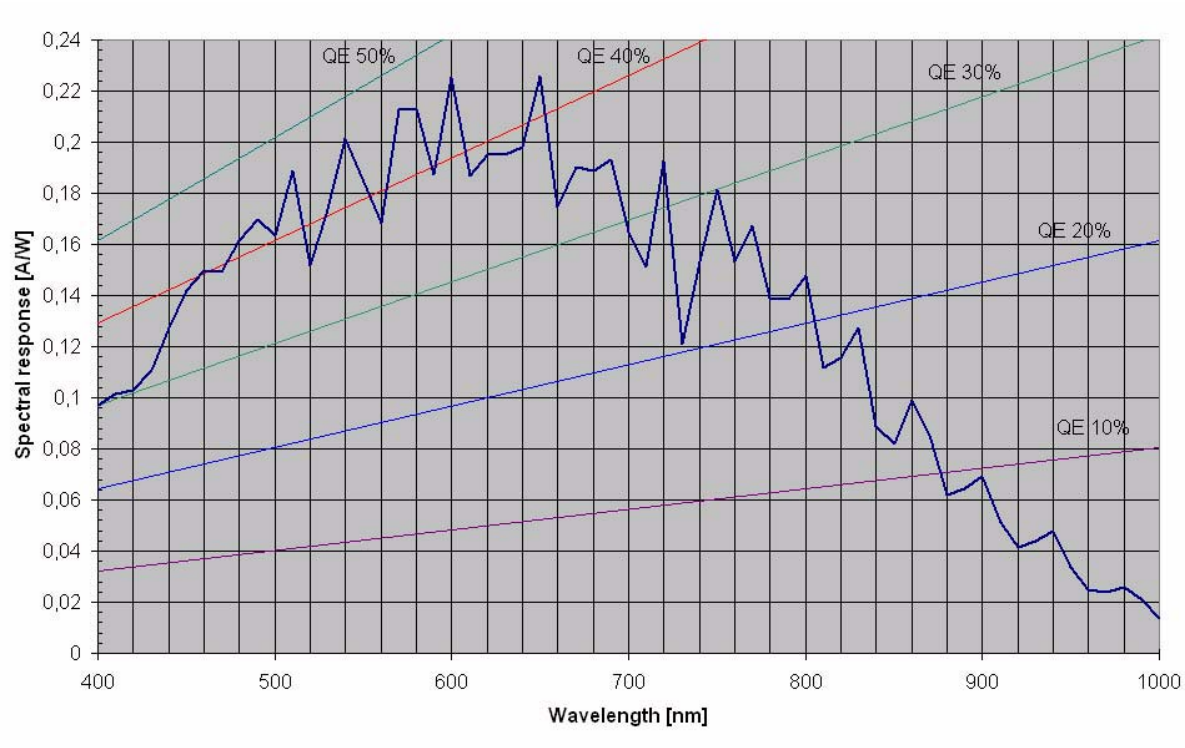
Table 10. IBIS4-14000 Electro-optical Specifications

Parameter	Value	Remarks
Effective conversion gain	18.5 V/e- 25 V/e-	Full range. See note 1. Linear range. See note 1.
Spectral response * fill factor	0.22 A/W (peak)	
Peak Q.E. * fill factor	45%	Between 500 and 700 nm.
Full Well charge	65000 electrons	See note 1.
Linear range	90% of full well charge	Linearity definition: < 3% deviation from straight line through zero point.
Temporal noise (kTC noise limited)	35 electrons	kTC noise, being the dominant noise source in the dark at short integration times.
Dynamic range	1857:1 (65.4 dB)	See note 1.
Linear dynamic range	1671:1 (64.5 dB)	See note 1; 3% deviation.
Average dark current	55 pA/cm^2	Average value @ 24°C lab temperature.
Dark current signal	223 electrons/s 4.13 mV/s	Average value @ 24°C lab temperature.
MTF at Nyquist	0.55 in X 0.57 in Y	Measured at 600 nm.
Fixed pattern noise (local)	0.11% Vsat RMS	Average value of RMS variation on local 32 x 32 pixel windows.
Fixed pattern noise (global)	0.15% Vsat RMS	
PRNU	<1% RMS of signal	
Anti-blooming	10^5	Charge spill-over to neighboring pixels (= CCD blooming mechanism)

Note
1. Settings: VDD = 3.3V, VDDR = 4V and VDD_ARRAY = 3V.

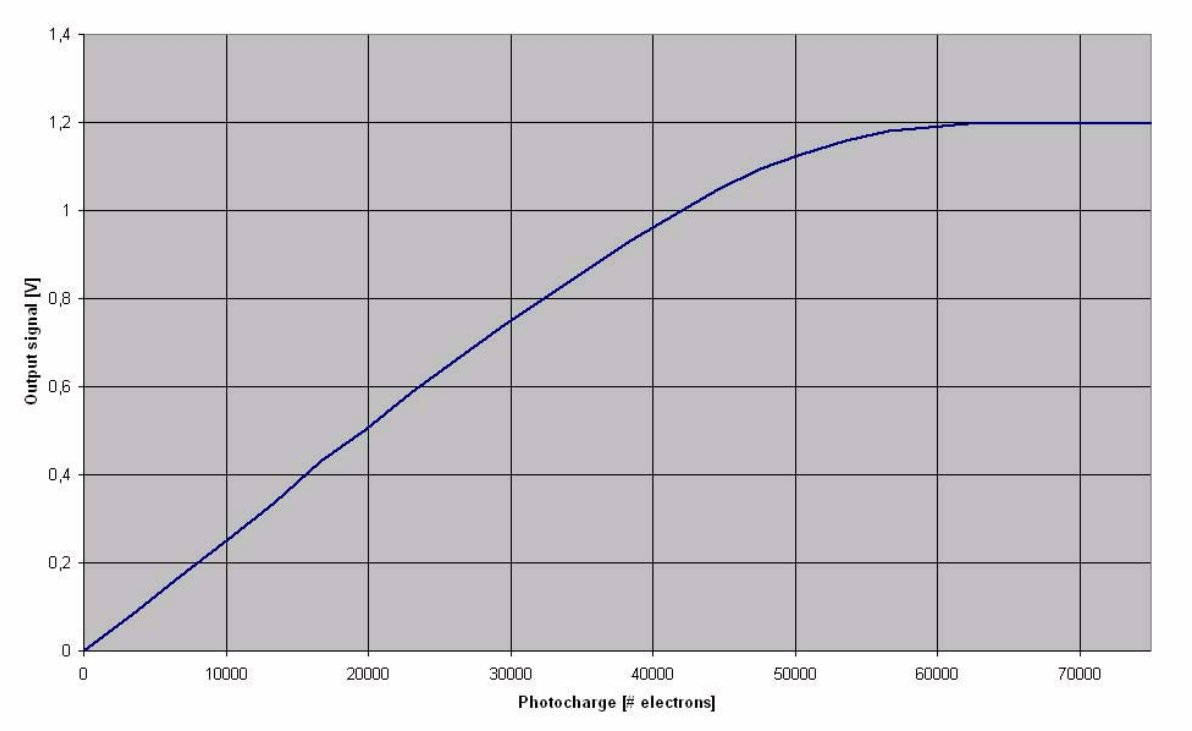
Spectral Response Curve

Figure 13. IBIS4-14000 Spectral Response Curve



Electro-voltaic Response Curve

Figure 14. IBIS4-14000 Electro-voltaic Response Curve



Electrical Specifications

Absolute Maximum Ratings

Table 11. IBIS4-14000 Absolute Maximum Ratings

Parameter	Description	Value	Unit
V_{DC}	DC supply voltage	–0.5 to +4.5	V
V_{IN}	DC input voltage	–0.5 to V_{DC} + 0.5	V
V_{OUT}	DC output voltage	–0.5 to V_{DC} + 0.5	V
I	DC current per pin; any single input or output	±50	mA
T_{STG}	Storage temperature range	–10 to 66 (@ 15% RH) –10 to +38 (@ 86% RH) (RH = relative humidity)	°C
Altitude		8000	feet

Recommended Operating Specifications

Table 12. IBIS4-14000 Recommended Operating Specifications

Parameter	Description	Min	Typ.	Max	Unit
VDD	Nominal power supply		3.3	3.6	V
VDDRL VDDRR	Reset power supply level		4		V
VDD_ARRAY	Pixel supply level		3		V
DARKREF	Dark reference offset level	1.7	2.65	3	V

Table 12. IBIS4-14000 Recommended Operating Specifications (continued)

Parameter	Description	Min	Typ.	Max	Unit
GNDAB	Anti-blooming ground level	0	0	1	V
V_{OUT}	Analog output level	0.5		3	V
V_{IH}	Logic input high level	2.5		3.3	V
V_{IL}	Logic input low level	0		1	V
T_A	Commercial operating temperature	0		50	°C (@ 15% RH)
T_A	Commercial operating temperature	0		38	°C (@ 86% RH)

Bias Currents and References

Table 13. IBIS4-14000 Bias Currents[2]

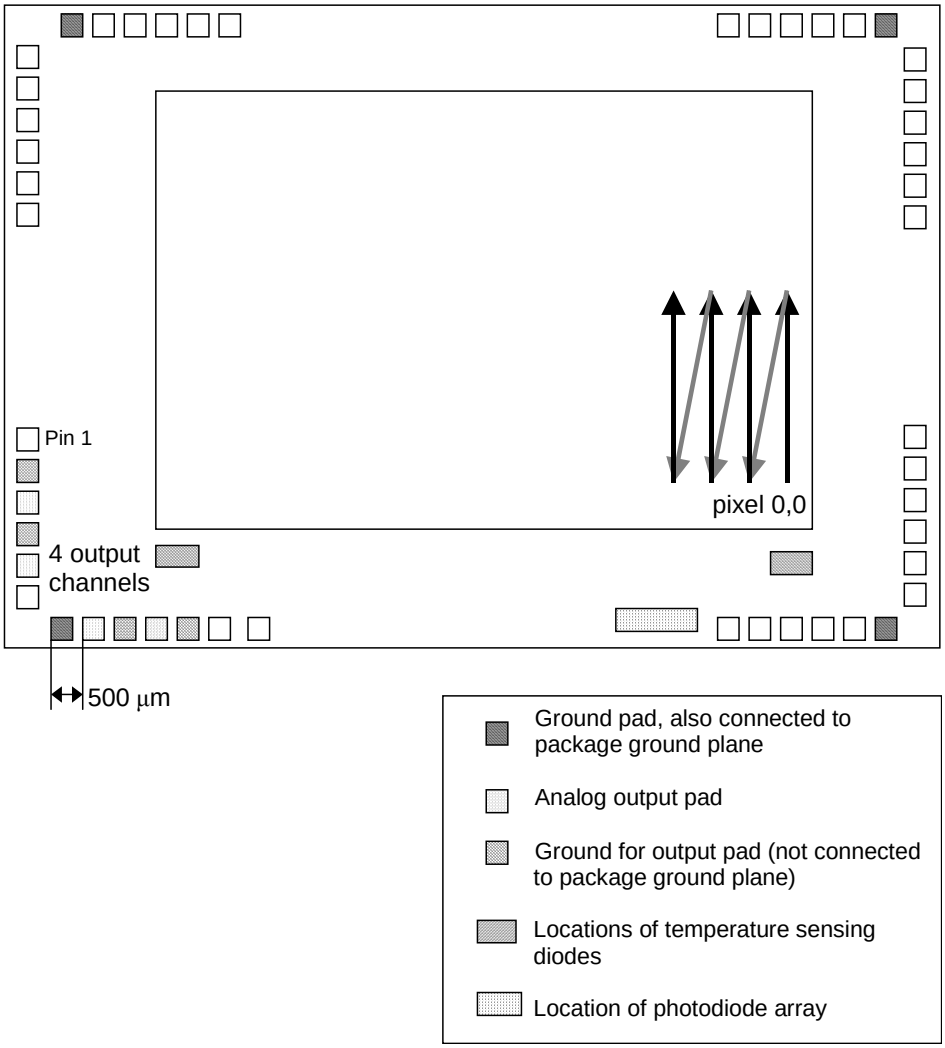
Pin Number	Pin Name	Connection	Input Current	Pin Voltage
1	OBIAS	10k to VDD	179 µA	1.51V
36	CBIAS	22k to VDD	91 µA	1.29V
37	PCBIAS	22k to VDD	91 µA	1.29V
48	XBIAS	10k to VDD	181 µA	1.49V
49	ABIAS	or 10M to VDD		0.8V

Note
2. Tolerance on bias reference voltages: ±150 mV due to process variances.

Geometry and Mechanical

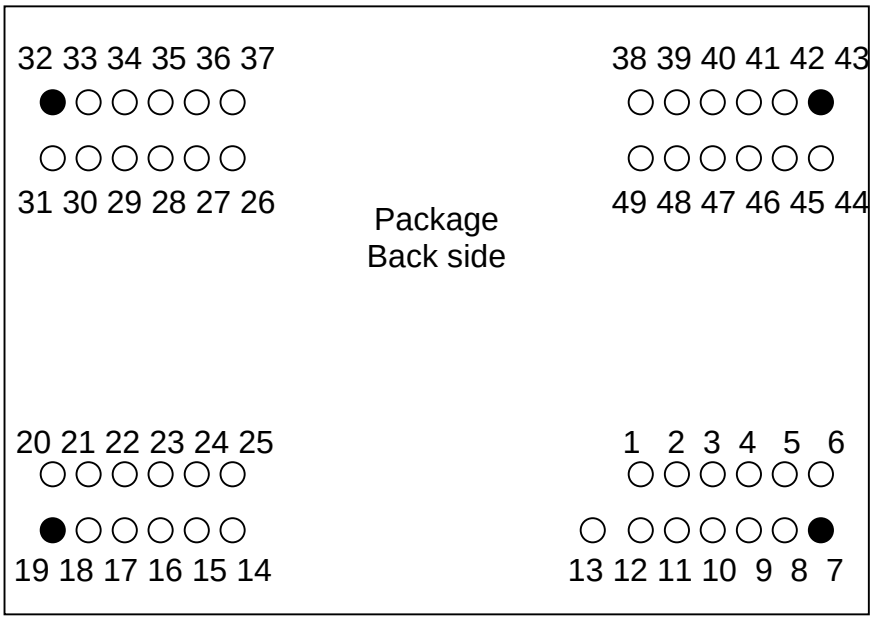
Die Geometry

Figure 15. Die Geometry and Location of Pixel (0,0)



Pin Number Assignment

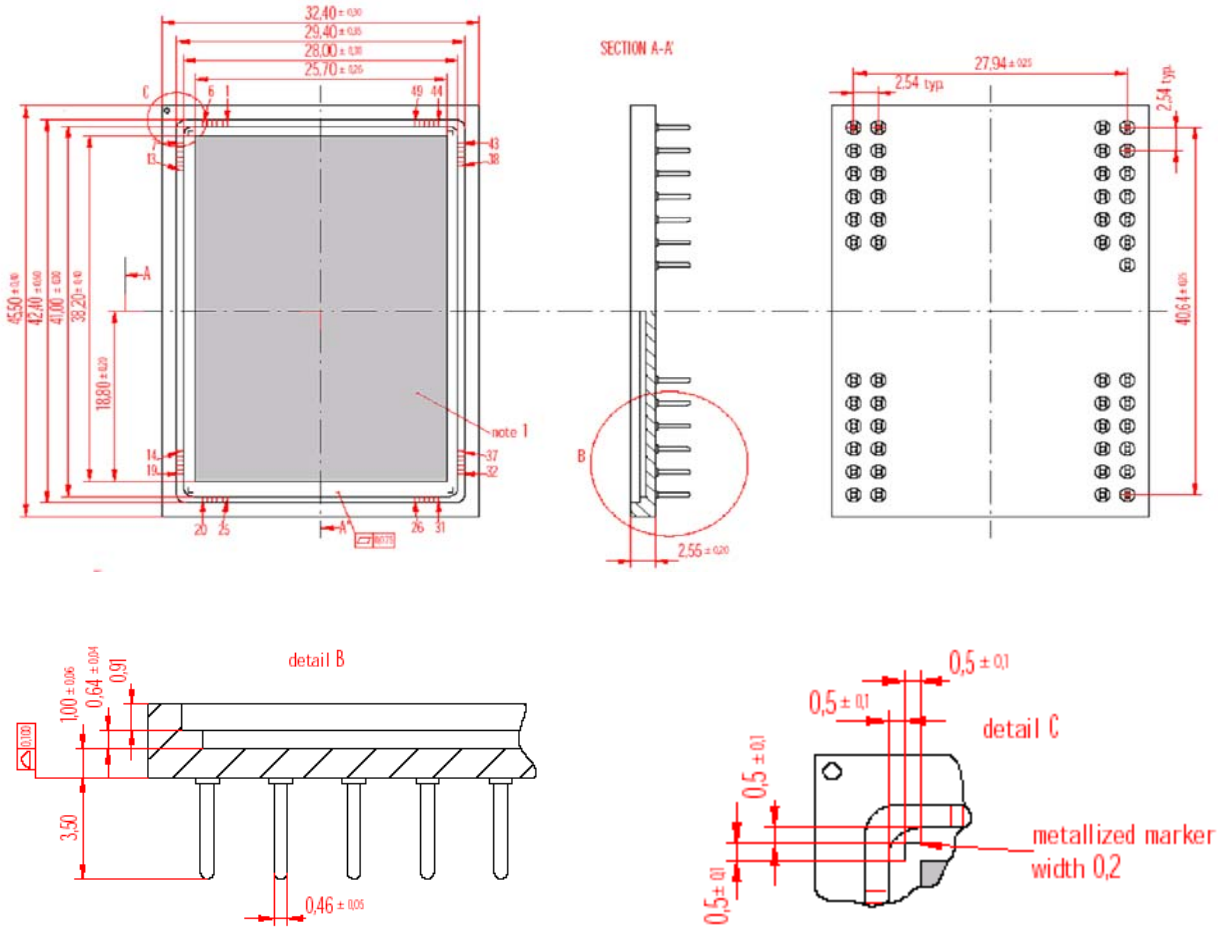
Figure 16. Pin Number Assignment



Note “Solid” drawn pins are connected to die attach area for a proper ground plane.

Elaborated Package Diagram

Figure 17. Package Dimensions



All dimensions are in mm

Based on 001-07577 *A

Die Placement Dimensions and Accuracy

Figure 18. Die Placement

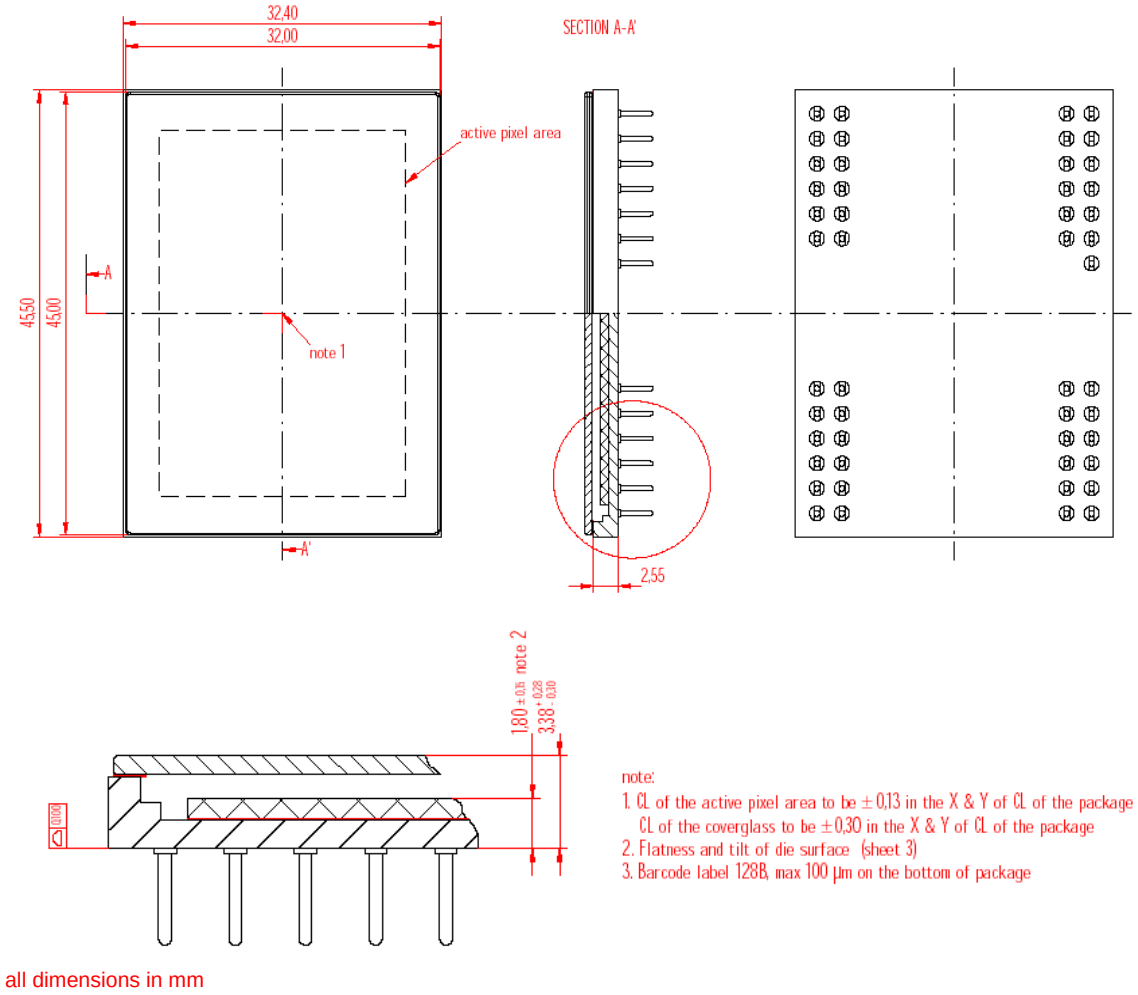
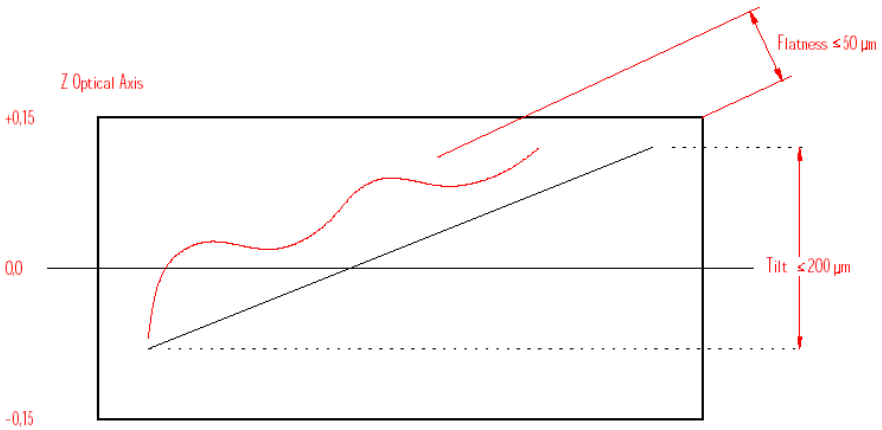


Figure 19. Tolerances

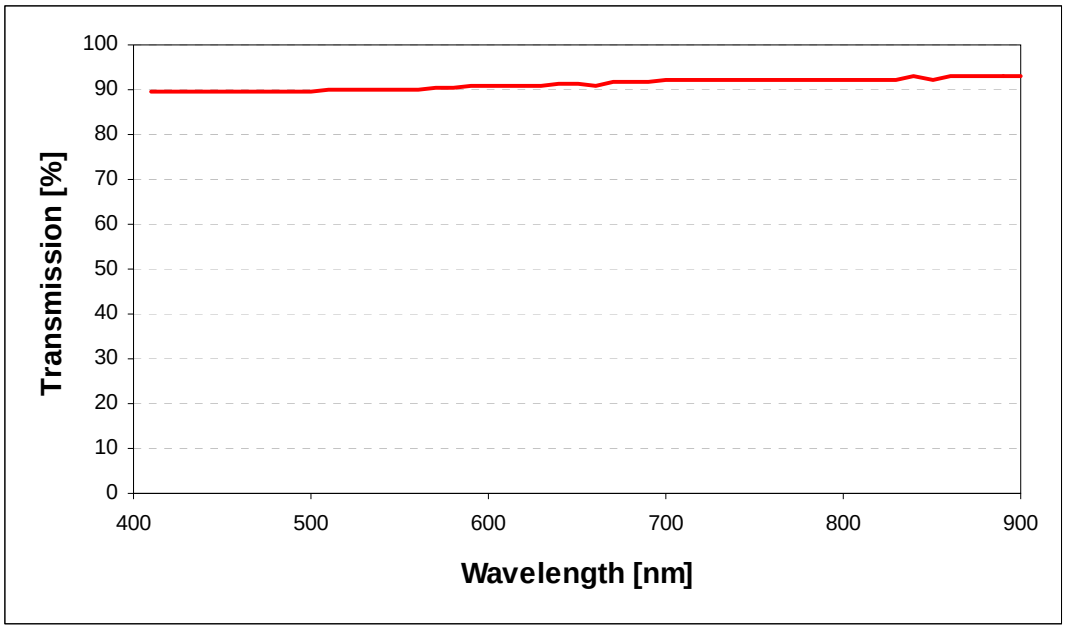


Cover Glass

CYII4SM014KAA-GEC (monochrome)

Schott D-263 plain glass is the cover glass of the IBIS4-14000 monochrome.

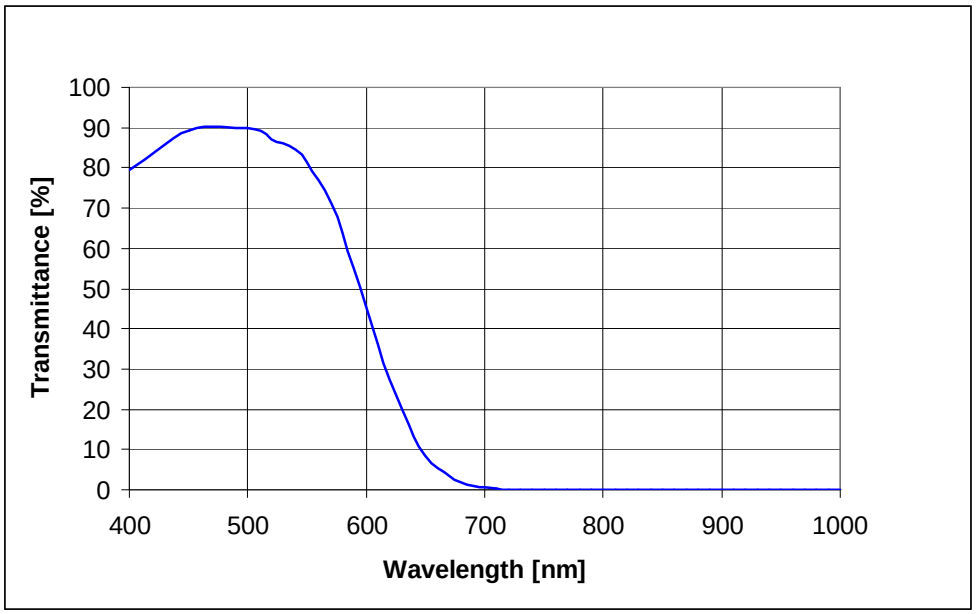
Figure 20. D-263 Transmittance Curve



CYII4SC014KAA-GTC (color)

S8612 glass is the cover glass of the IBIS4-14000 color.

Figure 21. S8612 Transmittance Curve (w/o AR coating)



Specification

- AR coating: 400–690 nm R < 1.5%
- Dig, haze, scratch 20 µm after coating
- Substrate: Schott S8612 glass
- Thickness: 0.7 mm ±0.050 mm
- Size: 31.9 x 44.9 mm^2 ±0.2 mm

Defects (digs, scratches) are detected at final test using F/11 light source. Glass defects that do not generate non correctable pixels are accepted.

Storage and Handling

Storage Conditions

Description	Minimum	Maximum	Unit	Conditions
Temperature	–10	66	°C	@ 15% RH
Temperature	–10	38	°C	@ 86% RH

Note: RH = Relative Humidity

Handling Precautions

Special care should be taken when soldering image sensors with color filter arrays (RGB color filters) onto a circuit board becasue color filters are sensitive to high temperatures. Prolonged heating at elevated temperatures can result in deterioration of the performance of the sensor. The following recommendations are made to ensure that sensor performance is not compromised during users' assembly processes.

ESD

Though not as sensitive as CCD sensors, the IBIS4-14000 is vulnerable to ESD like other standard CMOS devices. Device placement onto boards must be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Take into account standard ESD procedures when manipulating the device:

- Assembly operators should always wear all designated and approved grounding equipment. Grounded wrist straps at ESD protected workstations are recommended including the use of ionized blowers. All tools should be ESD protected. To ground the human body, provide a resistance of 1 MOhm between the human body and the ground to be on the safe side.
- When directly handling the device with the fingers, hold the part without the leads and do not touch any lead.
- To avoid generating static electricity:
  - ❒ Do not scrub the glass surface with cloth or plastic.
  - ❒ Do not attach any tape or labels.
  - ❒ Do not clean the glass surface with dust cleaning tape.
- When storing or transporting the device, put it in a container of conductive material.

Dust and Contamination

Dust or contamination of the glass surface can deteriorate the output characteristics or cause a scar. In order to minimize dust or contamination on the glass surface, take the following precautions:

- Handle the device in a clean environment such as a cleaned booth (the cleanliness should be, if possible, class 100).
- Do not touch the glass surface with the fingers.
- Use gloves to manipulate the device.

Soldering

Soldering should be manually performed with 5 seconds at 350°C maximum at the tip of the soldering iron.

Precautions and Cleaning

Avoid spilling solder flux on the cover glass; bare glass and particularly glass with anti reflection filters can adversely affected by the flux. Avoid mechanical or particulate damage to the cover glass. Avoid mechanical stress when mounting the device.

RoHS (Pb-free) Compliance

This section reports the use of Hazardous chemical substances as required by the RoHS Directive (excluding packing material).

Table 14. Chemical Substances and Information about Any Intentional Content

Chemical Substance	Any intentional content?	If there is any intentional content, in which portion is it contained?
Lead	NO	-
Cadmium	NO	-
Mercury	NO	-
Hexavalent chromium	NO	-
PBB (Polybrominated biphenyls)	NO	-
PBDE (Polybrominated diphenyl ethers)	NO	-

Information on lead free soldering

CYII4SM014KAA-GEC: The product is tested successfully for Pb-free soldering processes using a reflow temperature profile with maximum 260°C, minimum 40s at 255°C and minimum 90s at 217°C.

CYII4SC014KAA-GTC: The product will not withstand a Pb-free soldering process. Maximum allowed reflow or wave soldering temperature is 220°C. Hand soldering is recommended for this part type.

Note “Intentional content” is defined as any material demanding special attention is contained into the inquired product by following cases:

1. A case that the above material is added as a chemical composition into the inquired product intentionally in order to produce and maintain the required performance and function of the intended product .
2. A case that the above material, which is used intentionally in the manufacturing process, is contained in or adhered to the inquired product

The following case is not treated as “intentional content”:

1. A case that the above material is contained as an impurity into raw materials or parts of the intended product. The impurity is defined as a substance that cannot be removed industrially, or it is produced at a process such as chemical composing or reaction and it cannot be removed technically.

Ordering Information

Part Numbers

Table 15. Ordering Information

Part number	Package	Monochrome/Color	Glass lid
CYII4SM014KAA-GEC	49-pin PGA package	Monochrome	Monochrome
CYII4SC014KAA-GTC	49-pin PGA package	RGB Color	Color

Defect Specification

A document called “IBIS4-14000 Defect Specification” is available on request. This documents contains the criteria against which the IBIS4-14000 is tested before being shipped. Contact Cypress for more information (imagesensors@cypress.com).

Document History Page

Document Title: CYII4SC014KAA-GTC, CYII4SM014KAA-GEC IBIS4-14000 14-Megapixel CMOS Image Sensor Document Number: 38-05709			
REV.	**ECN NO.**	**Orig. of Change**	**Description of Change**
**	310213	SIL	Initial Cypress release
*A	428177	FVK	Layout converted Figure 10 on page 10 updated Storage and handling section added IBIS4-14000-C added
*B	642656	FPW	Ordering information update+package spec label. Moved figure captions to the top of the figures and moved notes to the bottom of the page per new template. Verified all cross-referencing. Moved the specifications towards the back. Corrected all variables on the Master pages.
*C	2220967	FPW	Eval kit section is removed. Reference to Defect Spec is added. Defect description for a RCCA added.